### ANALOG ELECTRONIC CIRCUITS (Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	10ES32	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

#### $\mathbf{PART} - \mathbf{A}$

#### **UNIT 1:**

**Diode Circuits:** Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clampers. **6 Hours** 

# **UNIT 2:**

**Transistor Biasing**: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization. **6 Hours** 

#### **UNIT 3:**

**Transistor at Low Frequencies:** BJT transistor modeling, CE Fixed biasconfiguration, Voltage divider bias, Emitter follower, CB configuration,Collector feedback configuration, Analysis of circuits  $r_e$  model; analysis ofCE configuration using h- parameter model; Relationship between h-parameter model of CE,CC and CE configuration.7 Hours

#### **UNIT 4:**

Transistor Frequency Response: General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency effects. 7 Hours

#### PART – B

#### **UNIT 5:**

(a) General Amplifiers: Cascade connections, Cascode connections, Darlington connections. 3 Hours

(b) Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits. Design procedures for the feedback amplifiers. 4 Hours

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#### **UNIT 6:**

Power Amplifiers: Definitions and amplifier types, series fed class Aamplifier, Transformer coupled Class A amplifiers, Class B amplifieroperations, Class B amplifier circuits, Amplifier distortions. Designing ofPower amplifiers.7 Hours

# **UNIT 7:**

**Oscillators:** Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators. **6 Hours** 

## **UNIT 8:**

**FET Amplifiers:** FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks.

**6 Hours** 

#### **TEXT BOOK:**

1. **"Electronic Devices and Circuit Theory"**, Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9<sup>TH</sup> Edition.

#### **REFERENCE BOOKS:**

- 'Integrated Electronics', Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2<sup>nd</sup> Edition, 2010
- 2. **"Electronic Devices and Circuits",** David A. Bell, PHI, 4<sup>th</sup> Edition, 2004
- 3. "Analog Electronics Circuits: A Simplified Approach", U.B. Mahadevaswamy, Pearson/Saguine, 2007.

#### LOGIC DESIGN (Common to EC/TC/EE/IT/BM/ML)

# Sub Code:10ES33IA Marks:25Hrs/ Week:04Exam Hours:03

**Exam Marks** 

:

100

UNIT 1:

**Total Hrs.** 

:

52

**Principles of combinational logic-1:** Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables,

PART – A

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