

## WORKING MODELS/CHARTS/MONOGRAMS, ETC

In order to ensure that the laboratory instructions are delivered more effectively, and to help the students use the equipment and technologies more easily, the department faculty members develop reference charts, in collaboration with professional designers. These charts are then printed and displayed in the laboratories, and help the students learn and effectively utilize the laboratory, during their curricular learning as well as their research and project work.

The following are some examples of Charts designed by the faculty, which are on display in the laboratories

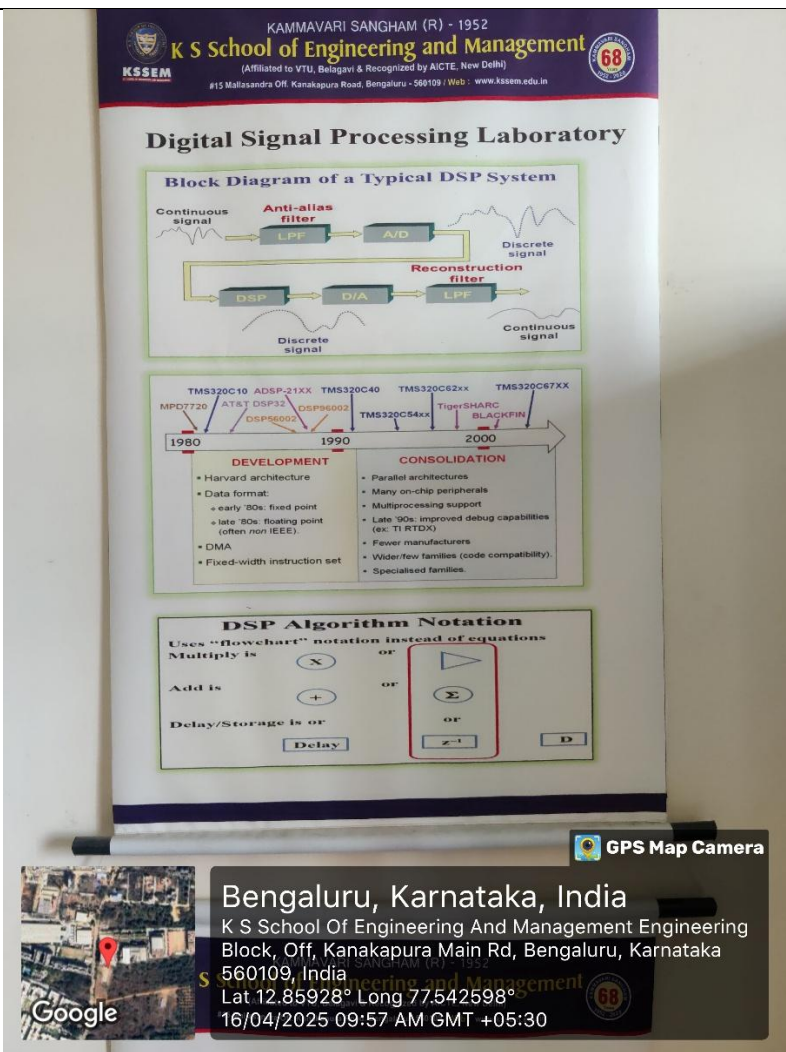
Sl No	Laboratory Name	Charts with Description
1	Digital Signal Processing Laboratory	 <p>The chart is titled "Digital Signal Processing Laboratory" and is from K S School of Engineering and Management. It features three main sections:</p> <ul style="list-style-type: none"> <li><b>Block Diagram of a Typical DSP System:</b> Shows a continuous signal entering an Anti-alias filter (LPF), then an A/D converter, resulting in a discrete signal. This discrete signal passes through a DSP block, then a D/A converter, and finally a Reconstruction filter (LPF) to produce a continuous signal.</li> <li><b>Evolution of DSP Processors:</b> A timeline from 1980 to 2000. <ul style="list-style-type: none"> <li><b>1980 (DEVELOPMENT):</b> Includes TMS320C10, ADSP-21XX, TMS320C40, and MPD7720. Characteristics include Harvard architecture, Data format, early '80s fixed point, late '80s floating point (often non IEEE), DMA, and Fixed-width instruction set.</li> <li><b>1990 (CONSOLIDATION):</b> Includes TMS320C62xx, TMS320C67XX, TMS320C54xx, and TMS320C60xx. Characteristics include Parallel architectures, Many on-chip peripherals, Multiprocessing support, Late '90s improved debug capabilities (ex: TI RTDX), Fewer manufacturers, Wider/few families (code compatibility), and Specialised families.</li> </ul> </li> <li><b>DSP Algorithm Notation:</b> Explains that it uses "flowchart" notation instead of equations. It defines symbols for Multiply (X), Add (+), Delay/Storage (Delay), and a combined block for Multiply, Add, and Delay (Σ, z⁻¹, D).</li> </ul> <p>At the bottom, a GPS Map Camera overlay shows the location: Bengaluru, Karnataka, India, K S School Of Engineering And Management Engineering Block, Off, Kanakapura Main Rd, Bengaluru, Karnataka 560109, India. It also provides coordinates (Lat 12.85928° Long 77.542598°) and a timestamp (16/04/2025 09:57 AM GMT +05:30).</p>

Fig 5.7.3.1: Typical DSP System, Evolution of DSP Processors



Fig 5.7.3.2: 8051 Microcontroller

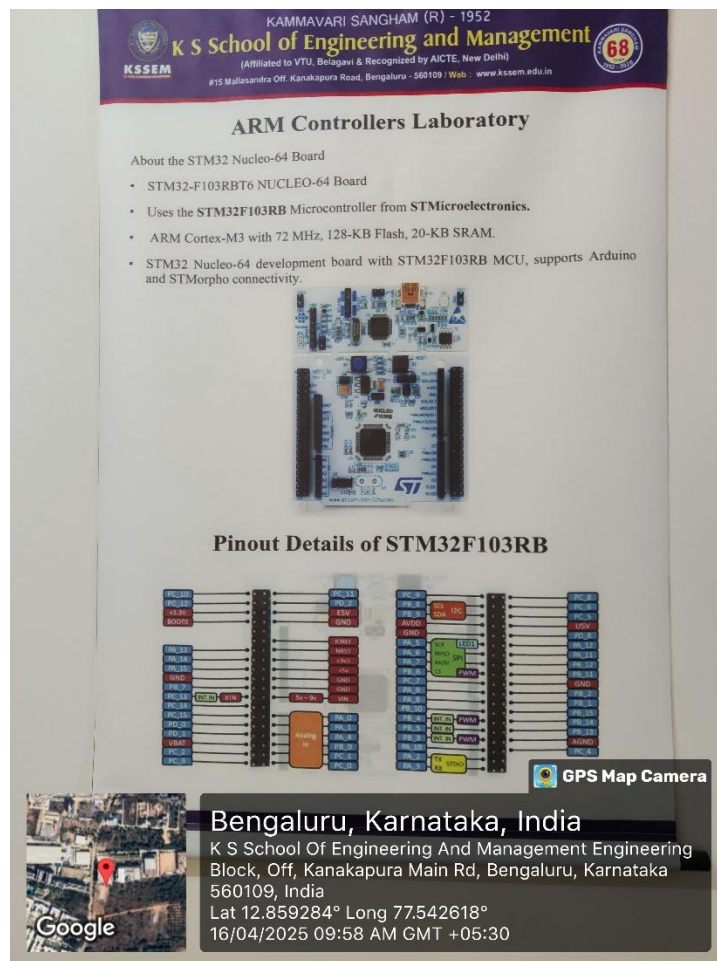


Fig 5.7.3.3: STM32F103RB Microcontroller

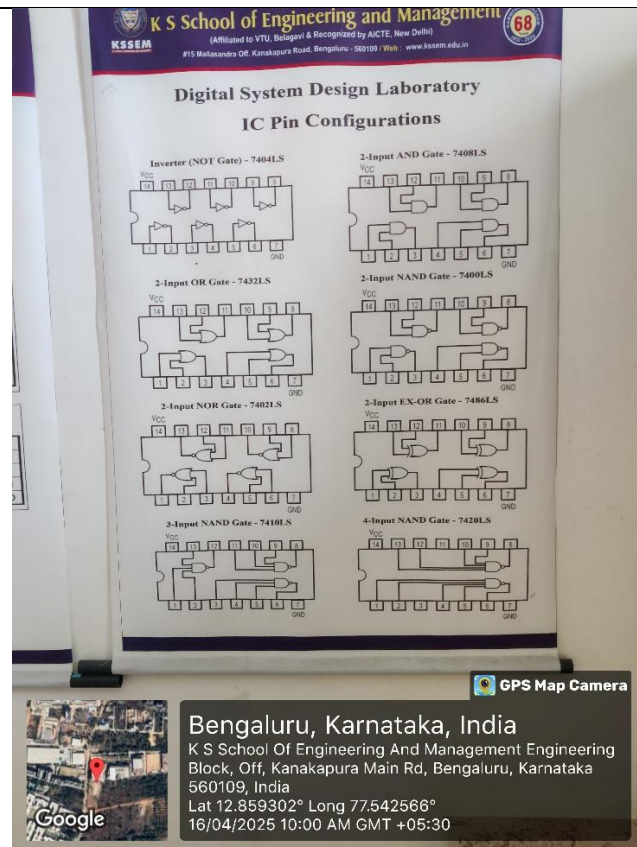


Fig 5.7.3.4: Commonly used Boolean Gate ICs

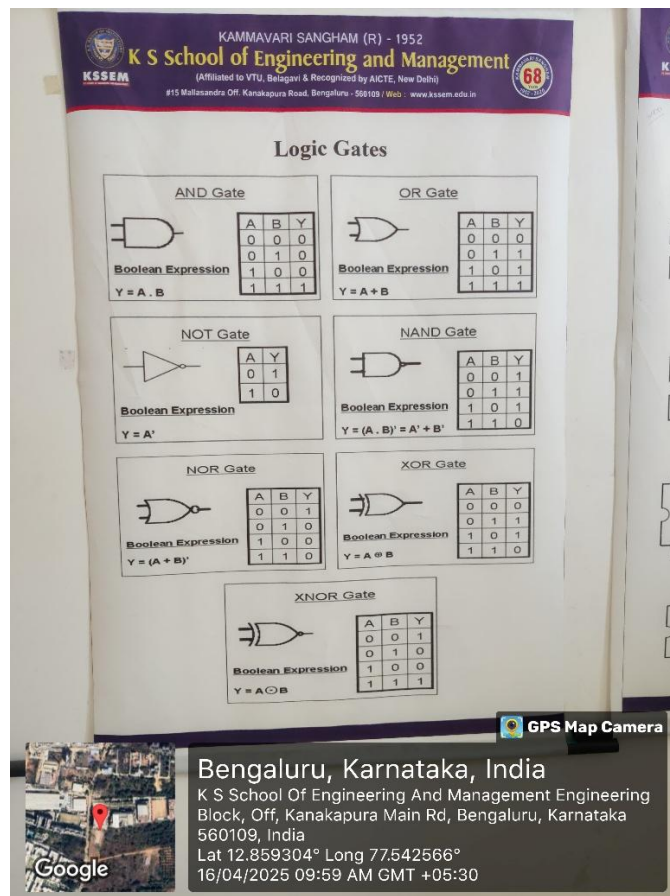


Fig 5.7.3.5: Basic Logic Gates for Digital Design



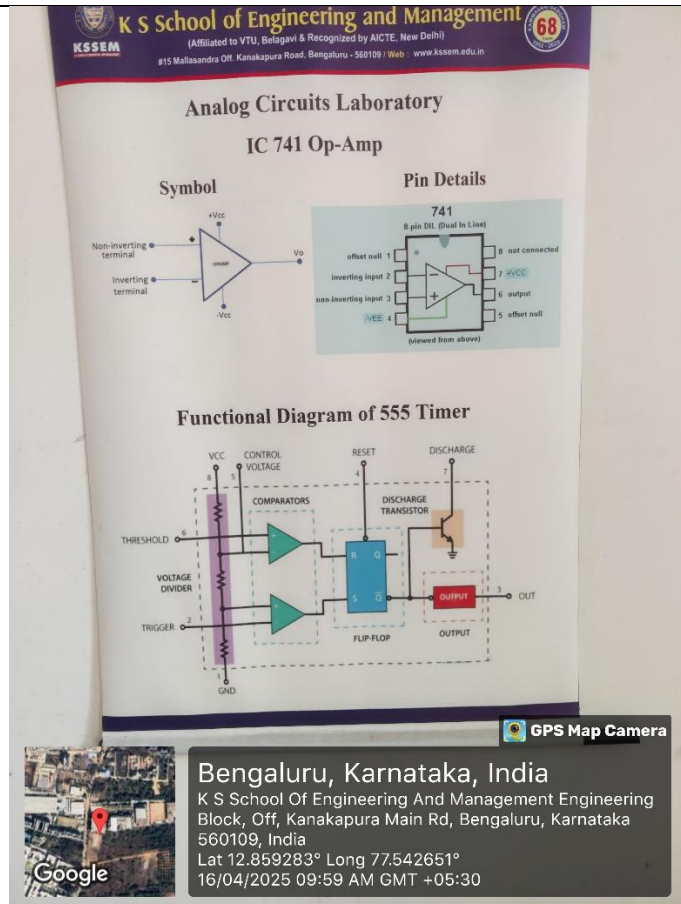


Fig 5.7.3.6: OpAmp IC 741, 55 Timer

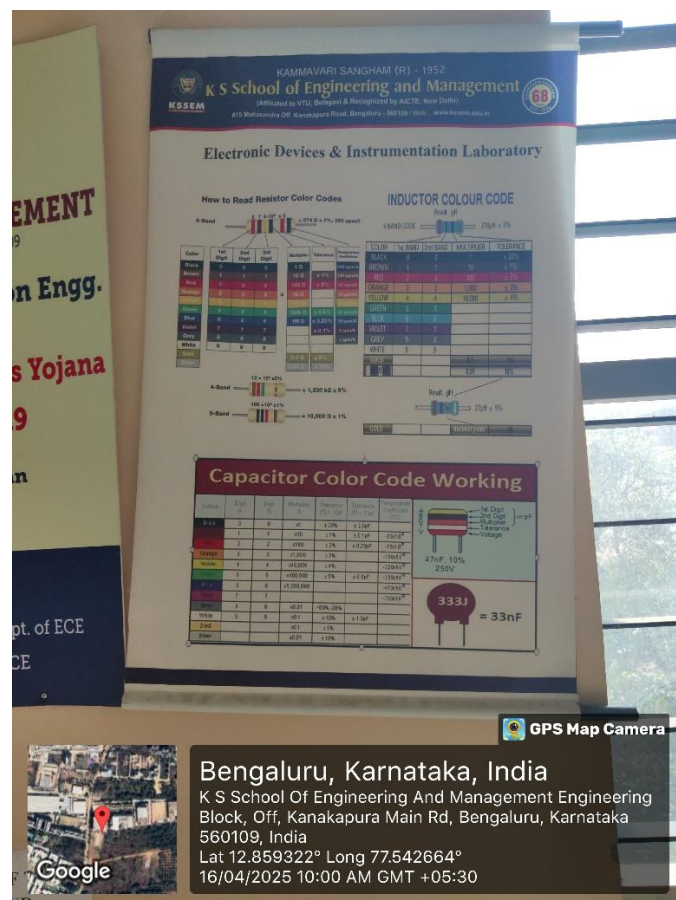


Fig 5.7.3.7: Resistance and Capacitance Colour Codes

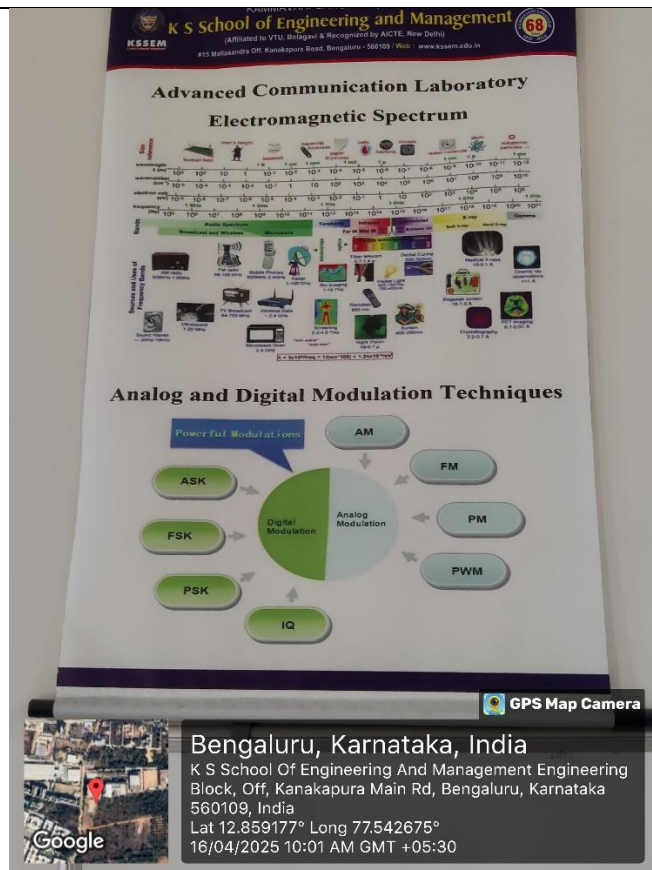


Fig 5.7.3.8: Moculation Techniques

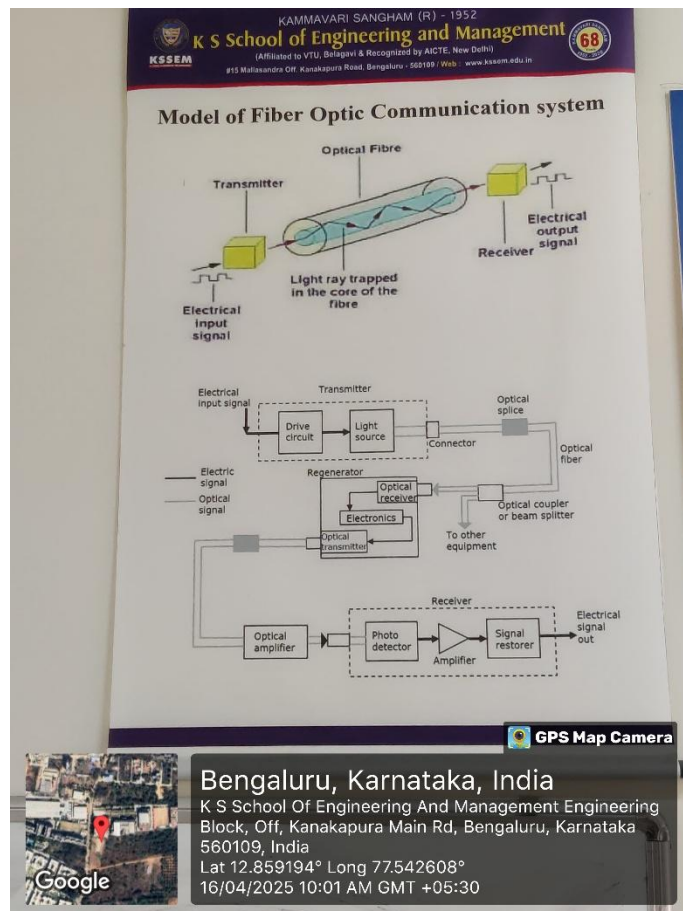


Fig 5.7.3.9: Fiber Optic Communication System

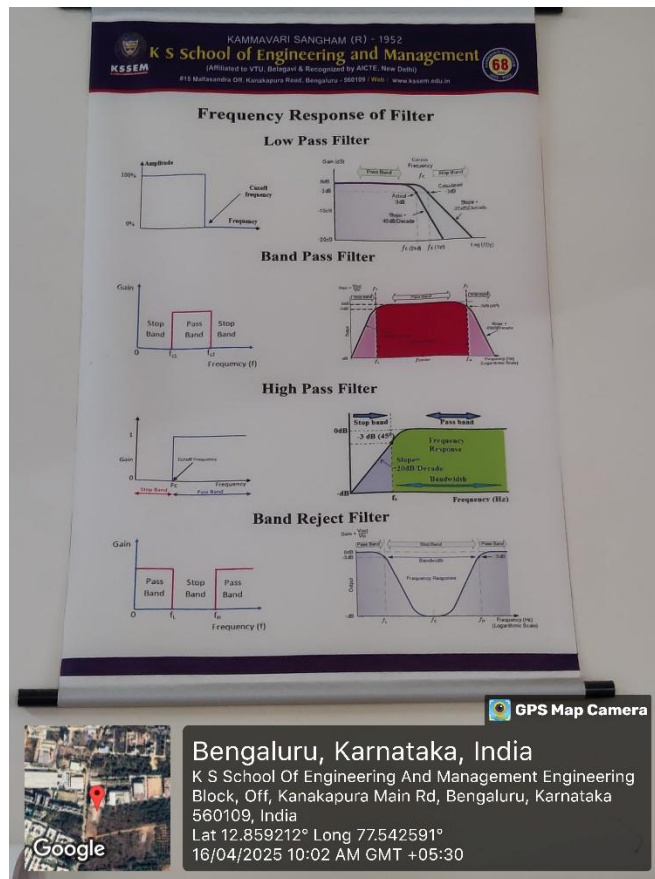


Fig 5.7.3.10: Filter Frequency Responses

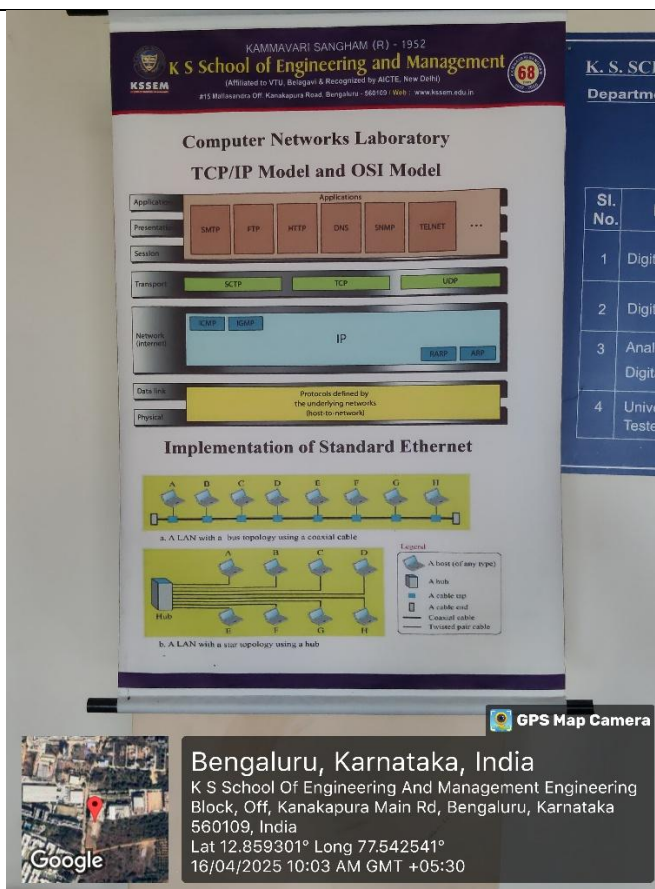


Fig 5.7.3.11: TCP/IP Models, Ethernet



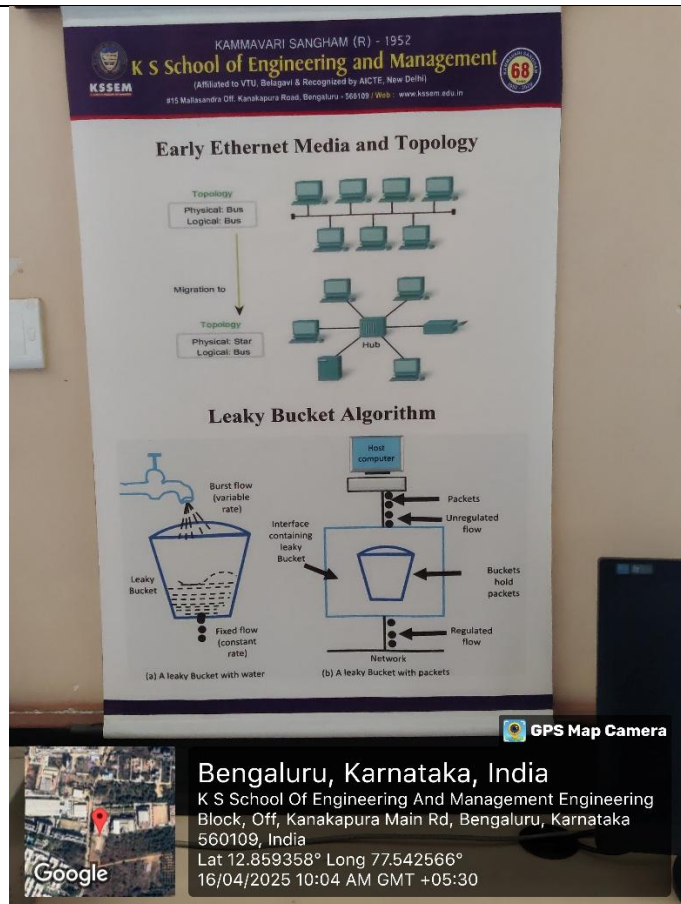


Fig 5.7.3.12: Network Topologies, Leaky Bucket Algorithm

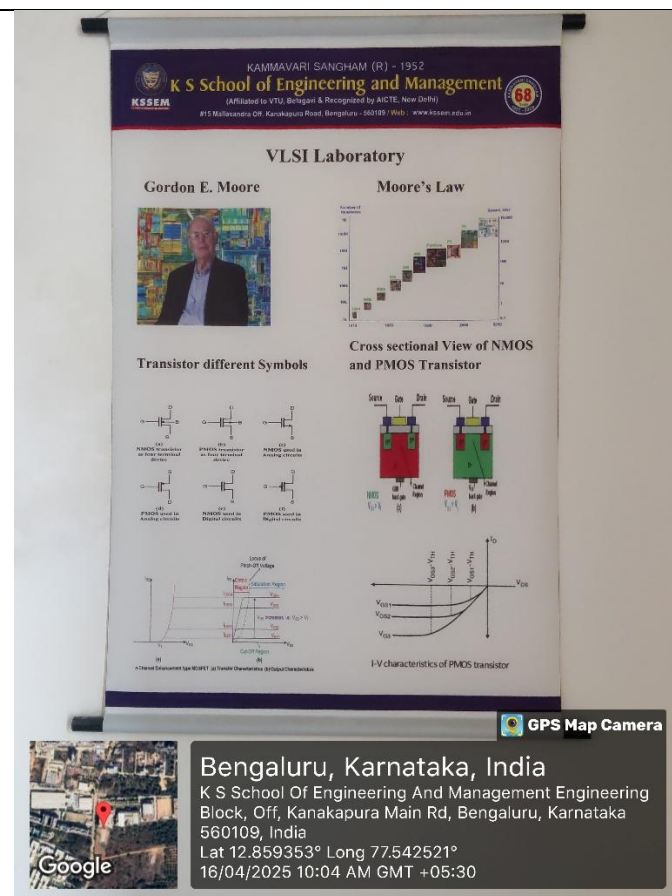


Fig 5.7.3.13: Moore's Law, Transistor Symbols, Structures

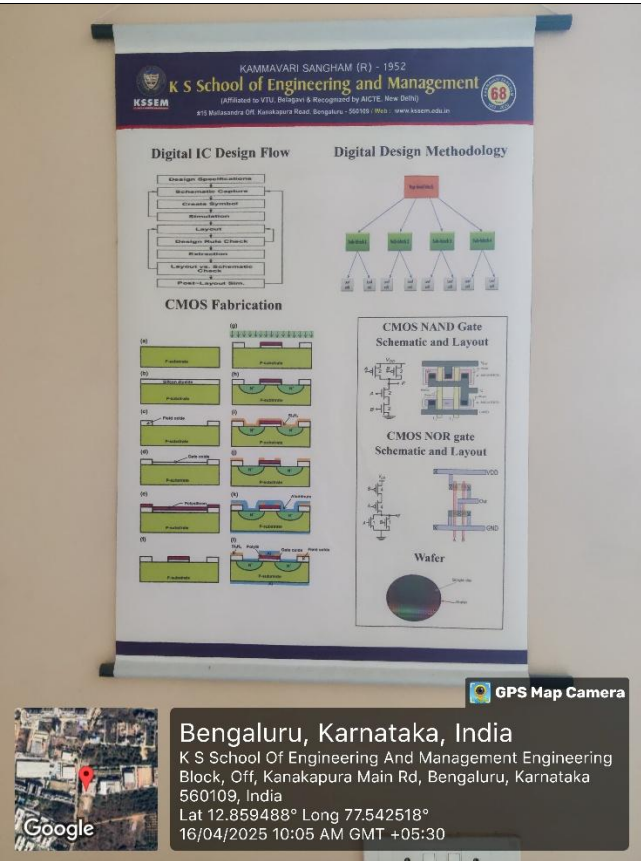
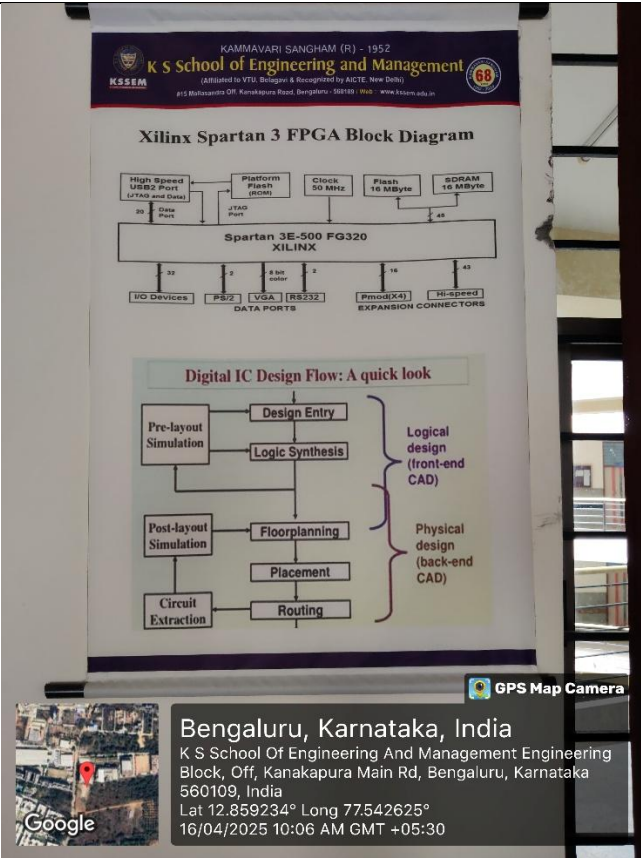
		 <p><b>Digital IC Design Flow</b></p> <p><b>Digital Design Methodology</b></p> <p><b>CMOS Fabrication</b></p> <p><b>CMOS NAND Gate Schematic and Layout</b></p> <p><b>CMOS NOR gate Schematic and Layout</b></p> <p><b>Wafer</b></p> <p><b>Bengaluru, Karnataka, India</b>  K S School Of Engineering And Management Engineering  Block, Off, Kanakapura Main Rd, Bengaluru, Karnataka  560109, India  Lat 12.859488° Long 77.542518°  16/04/2025 10:05 AM GMT +05:30</p>
7	HDL Laboratory	 <p><b>Xilinx Spartan 3 FPGA Block Diagram</b></p> <p><b>Digital IC Design Flow: A quick look</b></p> <p><b>Logical design (front-end CAD)</b></p> <p><b>Physical design (back-end CAD)</b></p> <p><b>Bengaluru, Karnataka, India</b>  K S School Of Engineering And Management Engineering  Block, Off, Kanakapura Main Rd, Bengaluru, Karnataka  560109, India  Lat 12.859234° Long 77.542625°  16/04/2025 10:06 AM GMT +05:30</p>

Fig 5.7.3.14: IC Design Methodology, CMOS Structures

Fig 5.7.3.15: IC Design Workflow, Xilinx Spartan 3 FPGA